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High Speed and Low Power Double-Tail Comparator using Switching Transistor

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Abstract: The high speed conversions are needed in the faster analog -to-digital converters. The accuracy of comparators is defined by its power consumption and speed. Many high speed ADCs, such as flash ADCs, require High speed, Low power comparators with small chip area. Conventional dynamic latched comparators suffer from low supply voltages especially when threshold voltage of the devices is not scaled at the same pace as the supply voltages of the modern CMOS process. The proposed comparator System has lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. In the dynamic Double tail comparator the simulation in a CMOS technology. In the Proposed dynamic Double tail comparator System both the power consumption and delay time will be significantly reduced. The maximum clock frequency of the proposed comparator can be reduced at modified supply voltages.

Keywords: CMOS, ADC, double tail, comparator.

I. INTRODUCTION

ADC uses comparators that compare reference voltages with the analog input voltage. When the analog voltage exceeds the reference voltage for a given comparator, a High is generated Dynamic latched comparators are very attractive for many applications such as high speed analog to digital converters (ADCs), memory sense amplifiers (SAs) and data receivers, due to fast speed, low power consumption, high input impedance and full swing output. They use positive feedback mechanism with one pair of back to back cross coupled inverters (latch) in order to convert a small input voltage difference to a full scale digital level in a short time. The demand of many ADCs, are high-speed, low power comparators with small chip area. In ultra deep sub micrometer (UDSM) CMOS high-speed comparators, the technology suffer from low supply voltages. This is severe especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that body driven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantizer for sub-1V modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to gmb of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In [7]–[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. In this paper the proposed double tail comparator is designed with a novel technique of using switching transistors.

II. REGENERATIVE COMPARATORS WITH CLOCK

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

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III. CONVENTIONAL AND DOUBLE TAIL COMPARATORS

A brief description of the conventional dynamic comparator and the double tail comparator are deal in this section

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A. Simple Conventional Dynamic Comparator

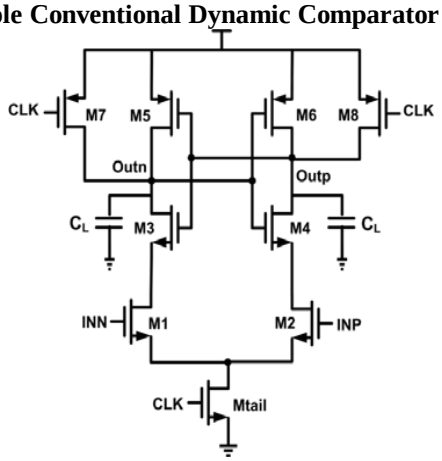

Fig. 1. Schematic diagram of the conventional dynamic comparator.

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and Mtail is off, reset transistors (M7–M8) pull both output nodes Outn and Outp to VDD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = VDD, transistors M7 and M8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp| before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP < VINN, the circuits works vice versa.

As shown in Fig. 1(b), the delay of this comparator is comprised of two time delays, t0 and tlatch. The delay t0 represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e., VINP > VINN), the drain current of transistor M2 (I2) causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current. Consequently, the discharge delay (t0) is given by

$$t_o = \frac{C_L|V_{thp}|}{I_2}$$

$$to \cong 2\frac{C_L|V_{thp}|}{I_{tail}} \qquad \text{- (1)}$$

In (1), since

$$I_2 = \frac{I_{tail}}{2} + \Delta I_{in} = \frac{I_{tail}}{2} + g_{m1,2}\,\Delta V_{in}$$

for small differential input (Vin), I2 can be approximated to be constant and equal to the half of the tail current.

The second term, tlatch, is the latching delay of two crosscoupled inverters. It is assumed that a voltage swing of Vout = VDD/2 has to be obtained from an initial output voltage difference V0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence, the latch delay time is given by

$$t_{latch} = \frac{C_L}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_o}\right) \qquad \text{- (2)}$$

Where gm,eff is the effective transconductance of the back-toback inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at t = t0). Based on (1), ΔV0 can be calculated from (3)

$$\Delta V_o = \left|V_{outp}(t = to) - V_{outn}(t = to)\right| \qquad \text{- (3)}$$

$$\Delta V_o = \left|V_{thp}\right| - \frac{I_2 t_o}{C_L}$$

$$\Delta V_o = \left|V_{thp}\right|\left(1 - \frac{I_2}{I_1}\right)$$

The current difference, ΔIin = |I1 − I2|, between the branches is much smaller than I1 and I2. Thus, I1 can be approximated by Itail/2 and (3) can be rewritten as

$$\Delta V_o = \left|V_{thp}\right|\frac{\Delta I_{in}}{I_1}$$

$$\Delta V_o \approx 2\left|V_{thp}\right|\frac{\Delta I_{in}}{I_{tail}} \qquad \text{-(4)}$$

$$\Delta V_o \cong 2\left|V_{thp}\right|\frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}}\Delta V_{in}$$

$$\Delta V_o = 2\left|V_{thp}\right|\sqrt{\frac{\beta_{1,2}}{I_{tail}}}\Delta V_{in}$$

In this equation, β1,2 is the input transistors current factor and Itail is a function of input common-mode voltage (Vcm) and VDD. Now, substituting V0 in latch delay expression and considering t0, the expression for the delay of the conventional dynamic comparator is obtained as

$$t_{delay} = t_o + t_{latch} \qquad \textbf{- (5)}$$

$$t_{delay} = 2\frac{C_L|V_{thp}|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \text{ X } \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right)$$

Equation (5) explains the impact of various parameters. The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input difference voltage (Vin). Besides, the delay depends indirectly to the input common-mode voltage (Vcm). By reducing Vcm, the delay t0 of the first sensing phase

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increases because lower Vcm causes smaller bias current (Itail). On the other hand, (4) shows that a delayed discharge with smaller Itail results in an increased initial voltage difference V0), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing of t0 and reducing of tlatch will finally lead to an increase in the total delay. In [17], it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower trans-conductances. Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. **Conventional Double-Tail Dynamic Comparator**

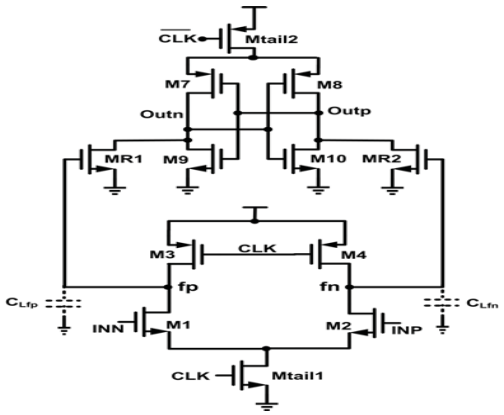

Fig. 2. Schematic diagram of the conventional double-tail dynamic comparator.

A conventional double-tail comparator is shown in Fig. 2 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10].

The operation of this comparator is as follows (see Fig. 2). During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage ΔVfn(p) will build up. The intermediate stage formed by MR1 and MR2 passes Vfn(p) to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t0 and tlatch. The delay t0 represents the capacitive charging of the load capacitance CLout (at the latch stage output nodes, Outn anOutp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thus t0 is obtained from

$$t_o = \frac{V_{Thn} C_{Lout}}{I_{B1}}$$
$$t_o \approx 2\frac{V_{Thn} C_{Lout}}{I_{tail2}} \quad \text{-(6)}$$

For the delay of the double-tail dynamic comparator, some important notes can be concluded. 1) The voltage difference at the first stage outputs (ΔVfn/fp) at time t0 has a profound effect on latch initial differential output voltage (ΔV0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator. 2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption.

C. **Latch Double Tail Dynamic Comparator**

Fig. 3 demonstrates the schematic diagram of the dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the comparator is to increase $\_V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner [see Fig. 3].

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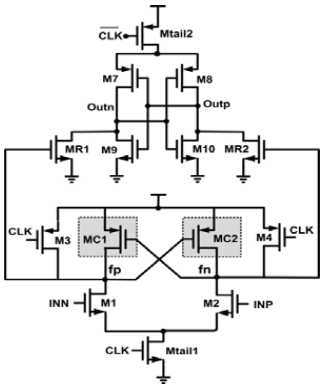


Fig. 3. Schematic diagram of the latch dynamic comparator Main idea.

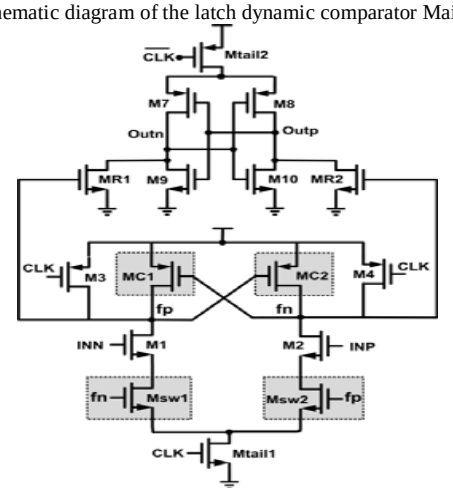
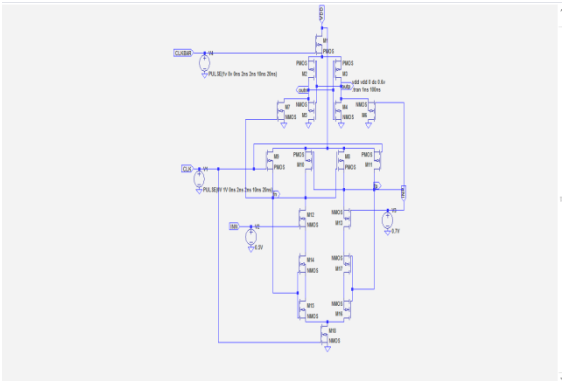


Fig. 4. Schematic diagram of the latch dynamic comparator Final structure.

The operation of the latch double tail comparator is as follows (see Fig4(b)). During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues falling, the corresponding pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which _*V*fn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (*M*c1) turns on, pulling the other node fp back to the *V*DD. Therefore by the time passing, the difference between fn and fp (_*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B). Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., *M*c1) turns on, a current from *V*DD is drawn to the ground via input and tail transistor (e.g., *M*c1, *M*1, and *M*tail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [*M*sw1 and *M*sw2, as shown in Fig. 4]. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to *V*DD for input voltage difference of _*V*in = 5 mV, *V*cm = 0.7 V, and *V*DD = 0.8 V. (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from *V*DD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

D. **proposed Dynamic Comparator**



Fig(4) Schematic diagram of proposed Dynamic Comparator.

Fig(4)Operation of modification in both reset and comparison phase is similar as proposed comparator .At the beginning of the decision making phase, both fn and fp nodes have been precharged to VDD. In the reset phase switches are closed , fn and fp starts to drop with different discharging rates. As soon as comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. fp is pulling up to VDD and fn should be discharged completely , hence switching in the charging path of fp will be opened but the other switch connected to fn will be closed to allow the complete discharge of fn node. The operation of the control transistors with the switches emulates the operation of the latch. t0(regeneration time).It can be achieved by designing first and second stage of tail currents. Low threshold pMOS devices can be used as control transistors leading to faster turn on in the fabrication technology. Another consideration is effect of mismatch between the controlling transistors of the comparator. In this modification mismatch effect is reduced. The large voltage variations in the internal nodes are coupled to the input disturbing the input voltage called

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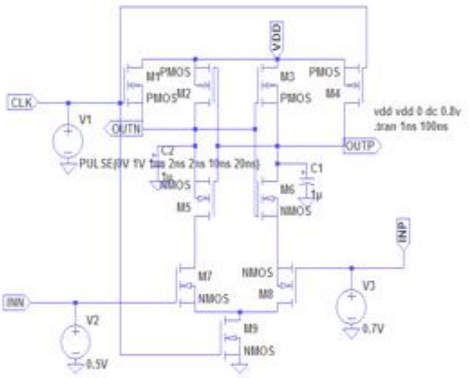
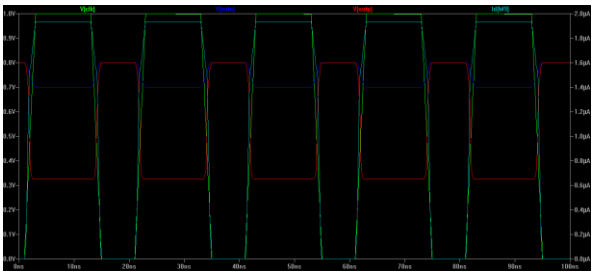
"kick back noise". Most efficient comparators generate this type of noise. The minimum kickback noise in the double tail comparator

IV. RESULTS

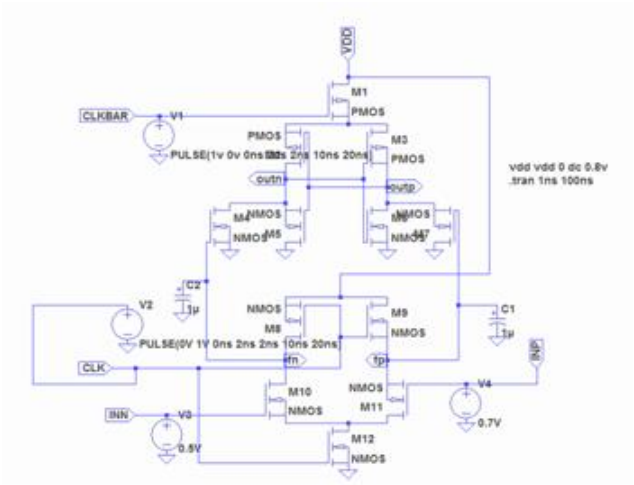
The results pertaining to the proposed technique are mentioned here in this sections. The schematic diagram followed by the output response for each model are presented subsequently here. The modelled schematic start from the conventional to the double tail comparator.



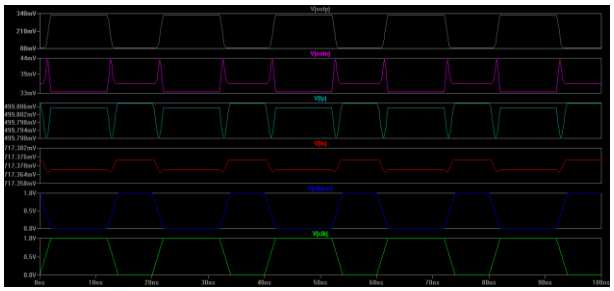


(c)

Fig 1 (a)Schematic diagram of the conventional dynamic comparator (b) model output waveform.

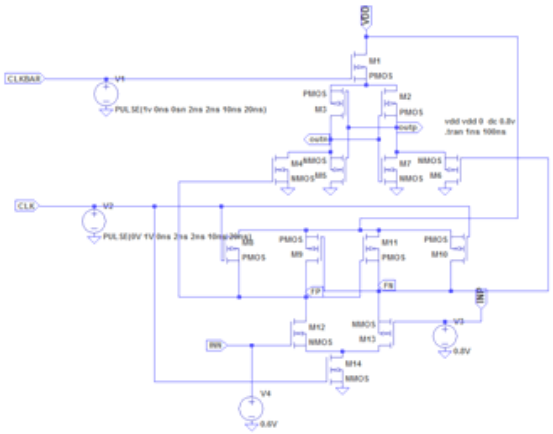


(a)



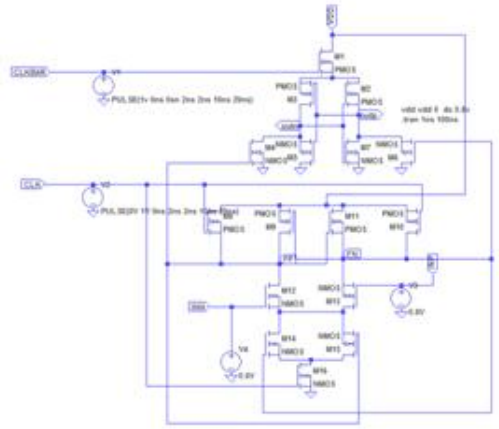
(b)

Fig 2 (a) Schematic diagram of the conventional double-tail dynamic comparator (b) Model Response

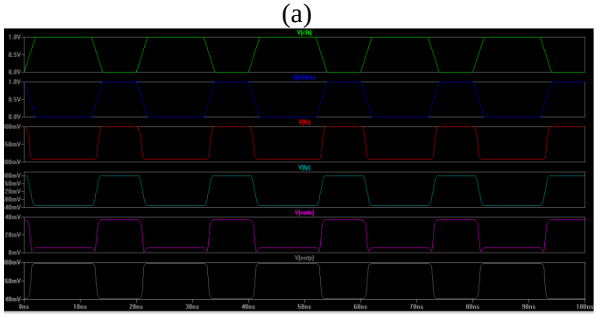


(a)

Fig 3 Schematic diagram of the latch dynamic comparator.



(a)



(b)

Fig 4(a) Schematic diagram of the latch dynamic comparator Final structure (b)output response.

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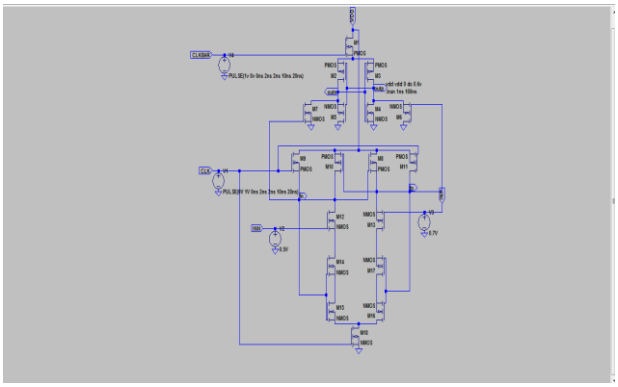
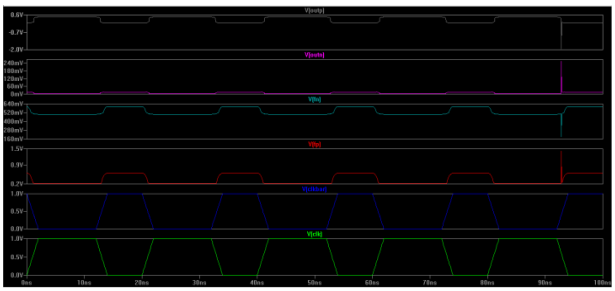


(a)



(b)

Fig 5(a) Schematic diagram of proposed Dynamic Comparator (b) output Response.

Table 1: Performance table

Comparator structure	Conventional dynamic comparator	Double tail dynamic comparator	Latch Double tail dynamic comparator	Proposed dynamic comparator
Technology CMOS	90nm	90nm	90nm	90nm
Supply voltage (V)	0.8	0.8	0.8	0.6
delay	66n	7.8n	7.6n	7.3n
Average Power	17µW	15µW	12µW	9µW
Area	16µ×16µ	28µ×12µ	28µ×14µ	28µ×16µ

V. CONCLUSION

Simulation of the conventional model and double tail models are presented in the section.IV. The response analysis based on the output waveforms are clearly mentioned in the corresponding waveform representation. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.09-µm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator. The performance of various comparators are tabulated and compared basing on various factors and parameters in table 1.

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